An FPGA-Based Focal Plane Array Interface for the Panchromatic Fourier Transform Spectrometer

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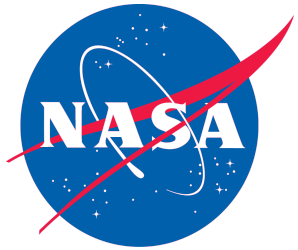

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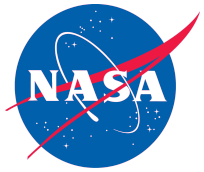

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Outline

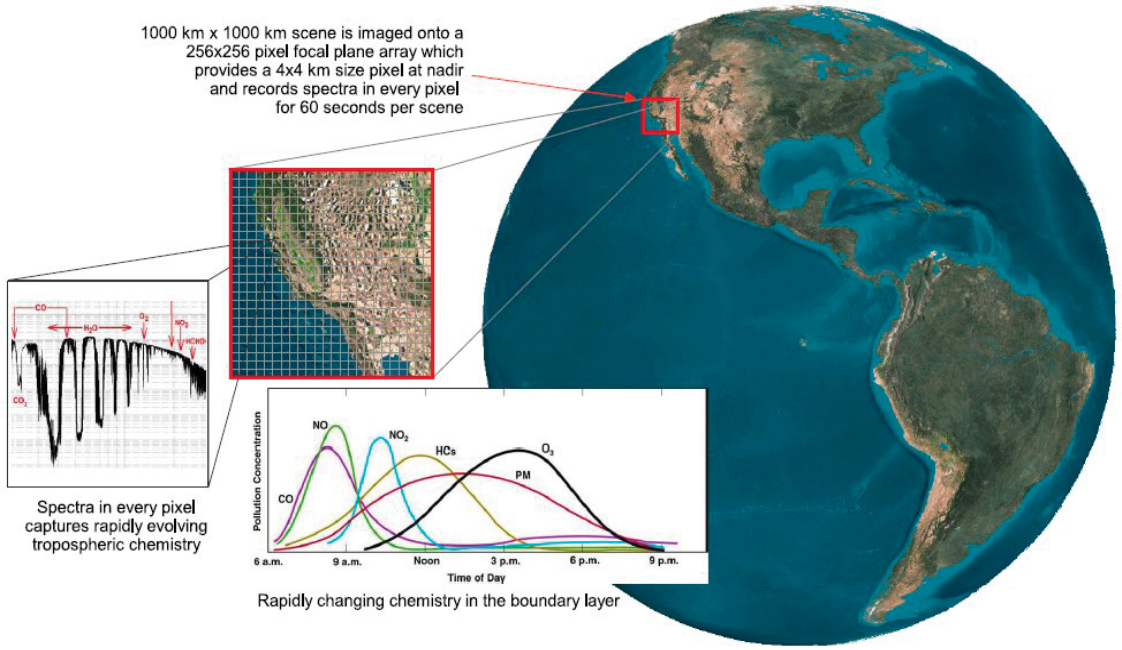
- The PanFTS Instrument
- Infrared Signal Chain Overview
- Data Acquisition System
- Troubleshooting
  - Networking bottlenecks
  - ADC clock skew
- Optical Layout
- Initial Results
- Current Progress
- Future work
- Conclusions

The PanFTS Instrument

- PanFTS is an Imaging Fourier Transform Spectrometer
  - Michelson interferometer (two in parallel)
    - "Camera" instead of traditional detector
    - Pictures recorded at high frame rates; path difference continuously varied
  - Fourier transform of each pixel recorded yields spectrum at observation
- Targeted for the Geostationary Coastal and Air Pollution Events (GEO-CAPE) mission – recommended by NRC Decadal Survey
- Up to four focal plane arrays (FPA) for IR and UV-Vis measurements
  - Goal: 256x256 pixels, 8kHz frame rate
  - Current progress: IR (Raytheon FPA) and UV-Vis (JPL developed)
  - Present capability: trades spatial coverage for frame rate
- FPGA and commercial ADCs control/gather data from FPAs

The PanFTS Instrument

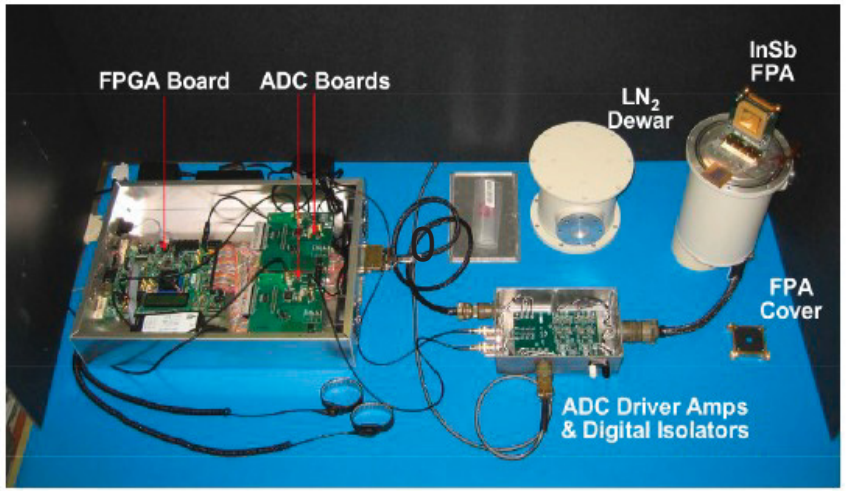
- Each of four cameras cover a 1000 km square scene at nadir
  - One minute scan time per scene
  - One hour cycle covering North and South America
- Key technology developments
  - High efficiency optical layout
  - Novel optical path difference mechanism
  - High frame rate FPAs
  - Processing elements to handle huge data rates

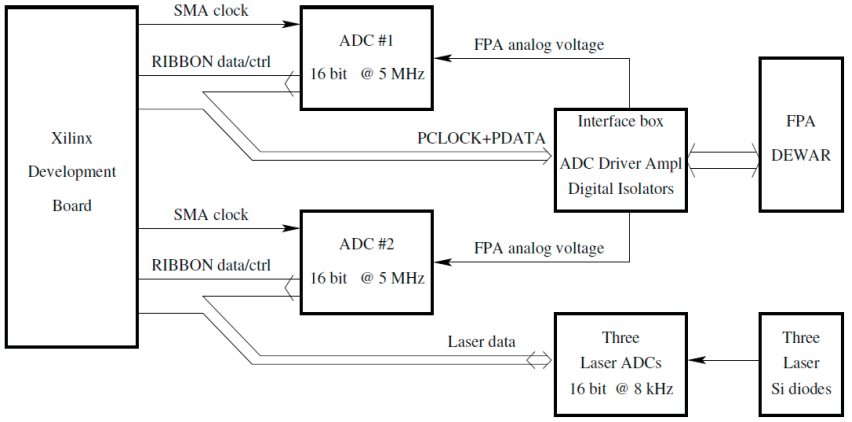


Imaging FTS observation scenario for GEO-CAPE mission

IR Signal Chain Overview

- Each FPA will generate data at 8 Gbit/sec (full resolution, full speed)
- Virtex-5 FPGA controls and processes data from FPAs
- IR signal chain consists of:
  - Xilinx ML507 development board
  - Raytheon FPA (InSb, LN_2 cooled)
  - Interface board for FPA
  - Dual Analog Devices ADC boards
  - Si reference laser detector, ADCs
- Reference laser used to perform re-sampling of FPA time-domain data to path-difference domain





IR signal chain

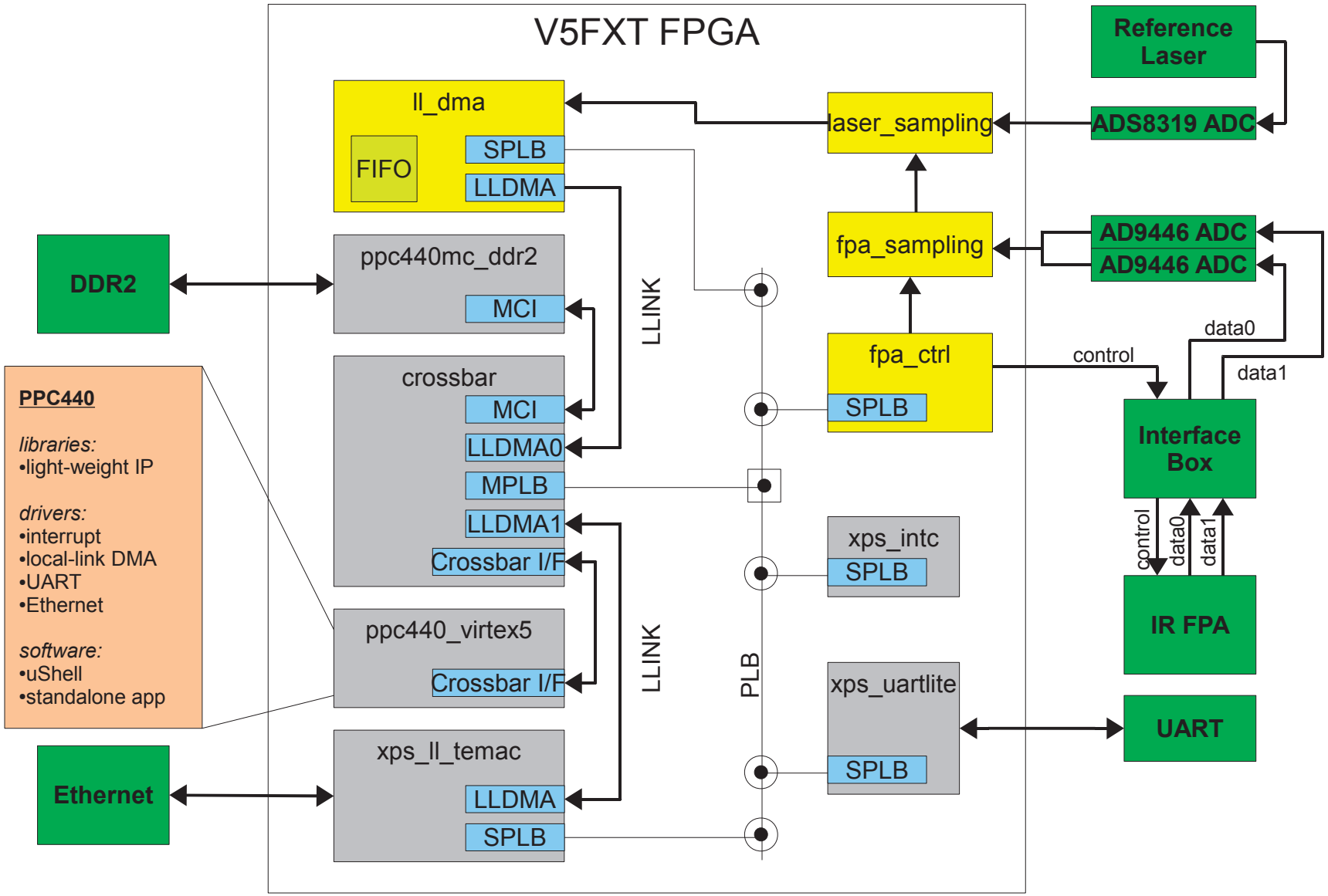
Data Acquisition System

- HW components (in FPGA fabric):
  - FPA controller sets FPA operation mode and window size
  - ADC samplers trigger conversions of FPA and reference laser signals; synchronize data stream
  - DMA engine passes data through FIFO buffer and autonomously transfers it to main system memory
- SW components (on embed. proc.):
  - Setup interrupts, DMA, peripherals
  - Configure FPA controller
  - Packetize captured data in main memory into TCP/IP frames
  - Run shell environment

Component	Loc	Type	Function
PowerPC 440	FPGA	HW	Sys processor
PLB v4.6	FPGA	HW	High speed sys bus
DDR2 SDRAM	FPGA	HW	Sys data memory
BRAM Ctrl	FPGA	HW	Sys instr memory
DMA Engine*	FPGA	HW	HW → MEM transfers
Interrupt Ctrl	FPGA	HW	Manage interrupts
Ethernet MAC	FPGA	HW	Eth PHY core
RS232 UART	FPGA	HW	User sys control
Clock Generator	FPGA	HW	Provides sys clks
FPA Ctrl*	FPGA	HW	IR FPA control
FPA Sampler*	FPGA	HW	IR ADC sampling
Laser Sampler*	FPGA	HW	Laser ADC sampling
Operating SW*	FPGA	SW	Main sys SW
uShell†	FPGA	SW	Minimalist shell
Lightweight IP	FPGA	SW	TCP/IP stack
TCP/IP Server	HOST	SW	Data recording on PC
Matlab Script*	HOST	SW	Real-time data plots

* These components were developed as part of the PanFTS IIP. The others in the table are provided by Xilinx or third parties.
† The uShell minimalist shell was developed by Thomas Werne at JPL.

Data Acquisition System

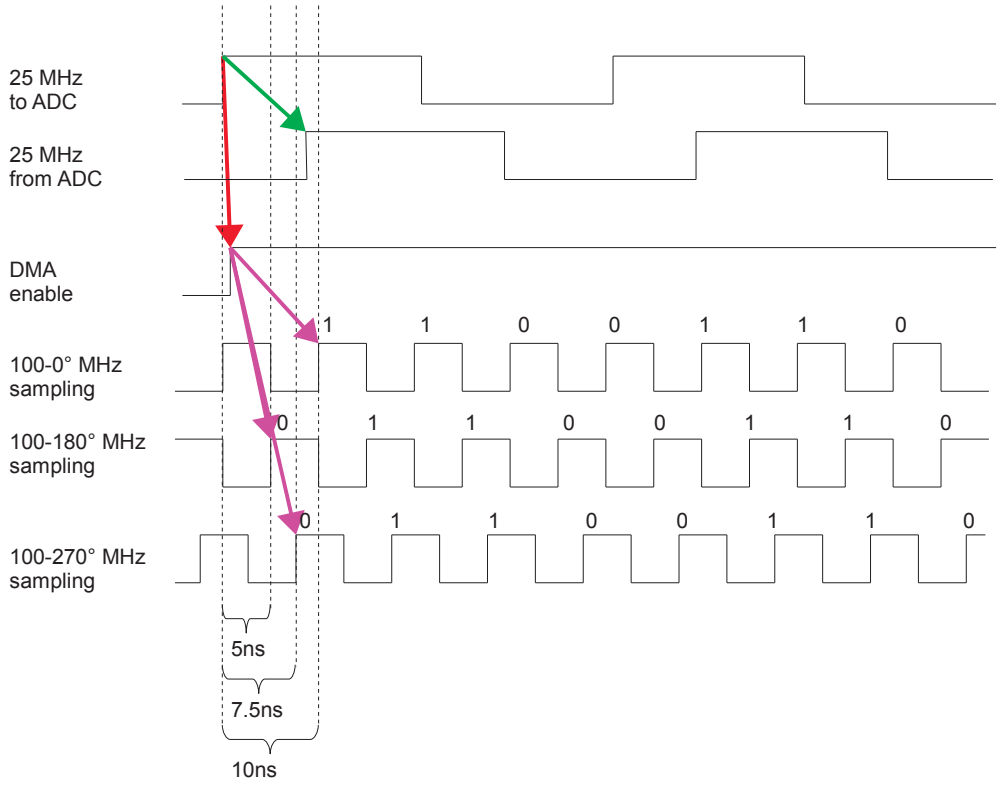


Troubleshooting - Networking

- Data is transferred off the FPGA to a host computer via Ethernet
  - Using Lightweight TCP/IP Stack (lwIP)
  - Significant load on CPU due to packetization overhead; dropped packets
- Improved performance by two means:
  - Relocation of instruction code from external DDR2 memory to internal BRAM
    - Leaves DDR2 memory only for data space and writing from DMA engine
    - Eliminates memory contentions for simultaneous data/instruction access
  - Explicitly flush data cache before packaging into TCP/IP packet
    - Removes stale content from data cache (due to autonomous DMA transactions)
    - Ensures next memory access pulls in new data into cache

Troubleshooting - Clock Skew

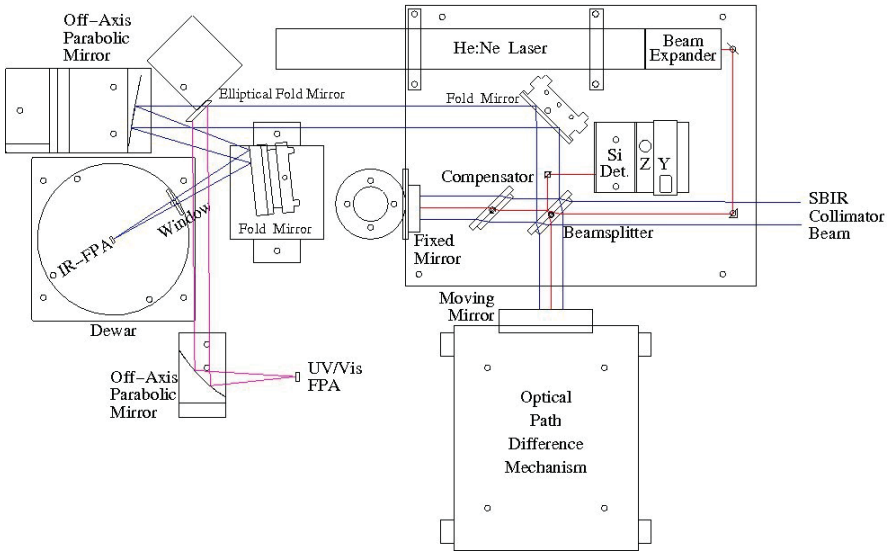
- Dual ADCs digitize FPA output
  - FPGA provides input clock
  - Delayed output clock returned by ADCs
- No clock-capable I/O readily available on ML507 board (for ADC interfacing)
- Solution: experimentally determine clock skew
  - Generate 25 MHz clock to ADCs
  - Sample return clock with 100 MHz clock
- Found that 180° phase delay is acceptable for sampling

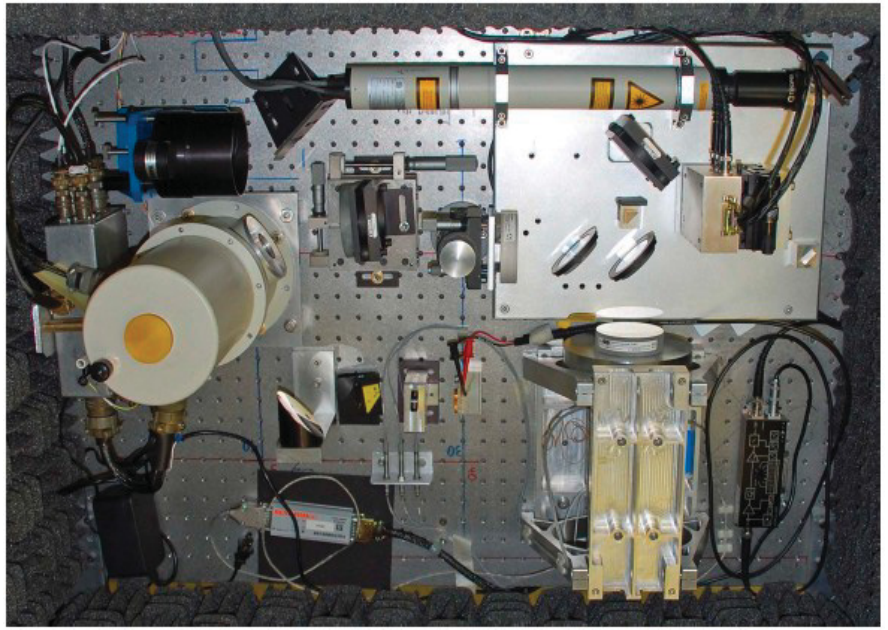


Clock skew test

Optical Layout

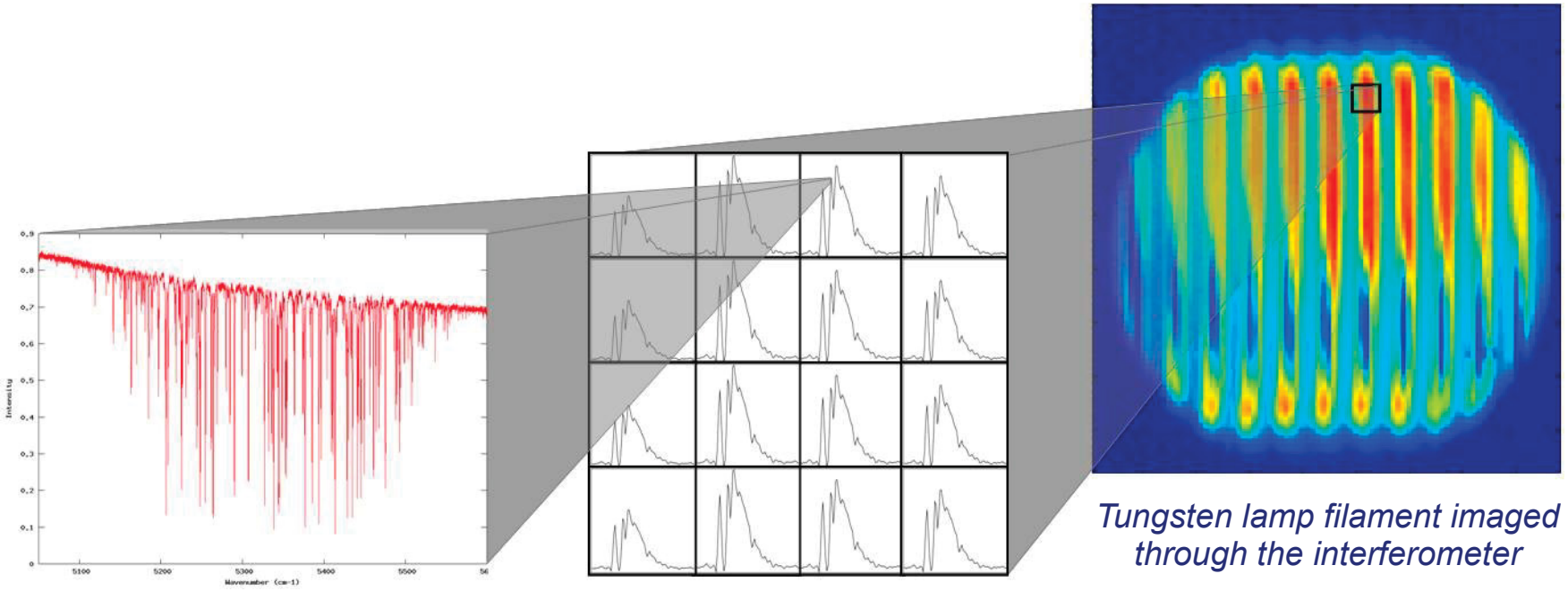
- Collimated beam illuminates PanFTS breadboard
  - Illumination source is a halogen lamp with wound tungsten filament
  - Filament is imaged onto circular stop in the field plane of the collimator
- Single-frequency laser serves as reference for conversion from time domain to optical path difference
- Light is modulated in intensity by optical path difference mechanism
  - Focused onto Raytheon IR FPA
  - Small portion is deflected to JPL UV-Vis detector





Initial Results

- First recording used a 88x88 pixel window to fit lamp filament
  - Frame rate: 767 Hz, Nyquist rate: 383 Hz
  - OPDM velocity set to make laser light appear at 376 Hz (just below Nyquist rate)
- Setup used as overall health check of the system

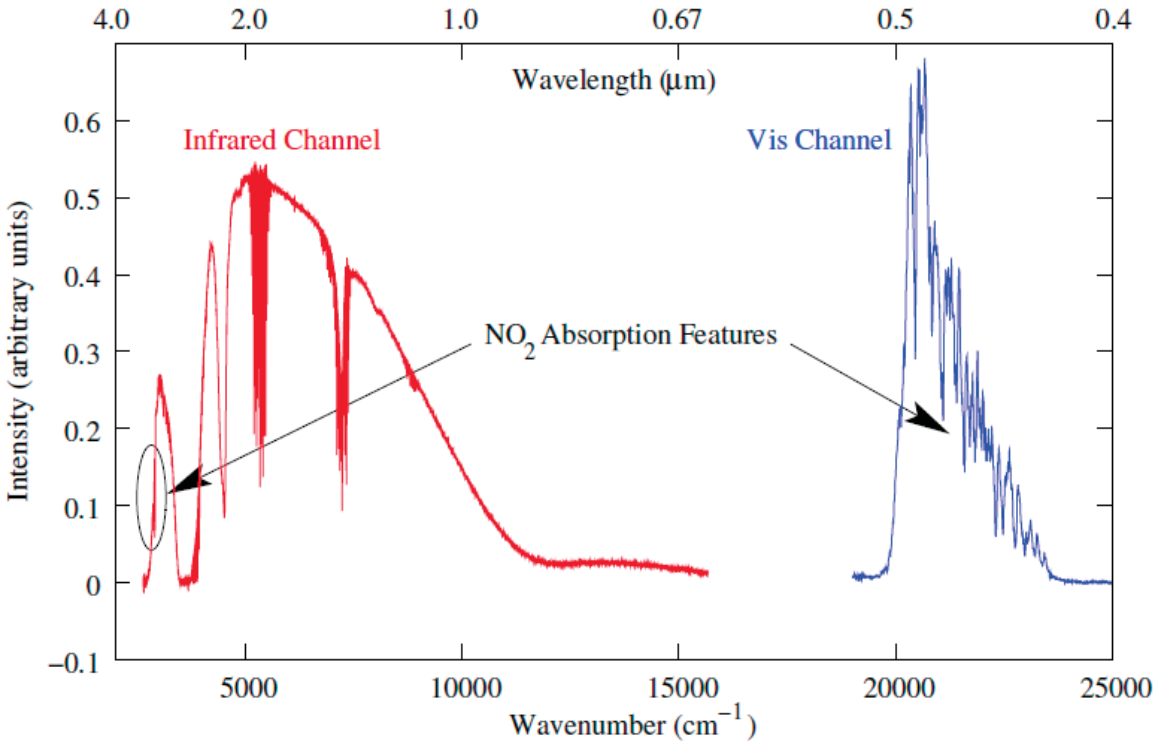


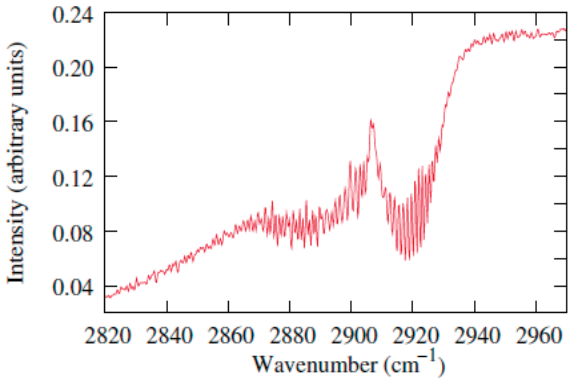
Tungsten lamp filament imaged through the interferometer

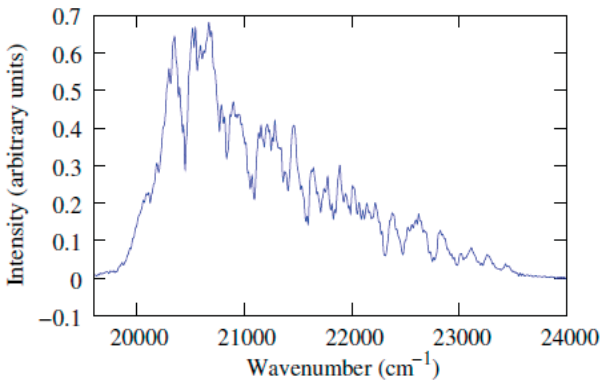
IR spectra in every pixel captured high resolution spectrum of the 1.9 µm water vapor band

Initial Results

- High speed recording: 8x8 window, 8.143 kHz frame rate
  - Increased OPDM scan velocity; laser appears at 2.633 kHz
  - In addition to Raytheon IR FPA, also used single-element UV-enhanced detector, recorded by commercial sigma-delta ADCs
- Placed NO_2 cell in light path; recorded IR, UV-Vis, laser interferograms

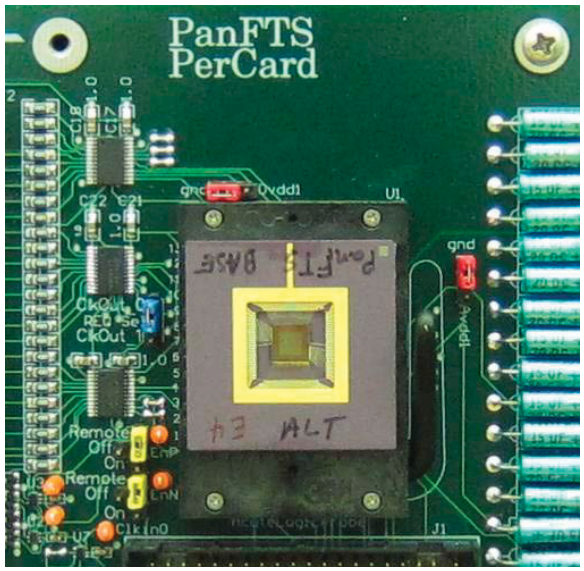




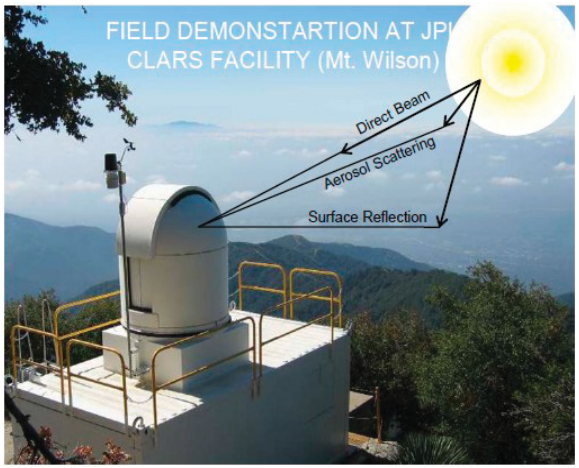


Current Progress

- Integration with JPL-developed sigma-delta read-out integrated circuit (ROIC)
  - ROIC bump-bonded to detector portion of UV-Vis FPA
  - Captured single-bit modulator output
  - Developing delta-sigma filtering IP core and integrating with FPGA data acquisition
- Working towards moving PanFTS to CLARS facility at Mt. Wilson
  - Improving user control software
  - Adding system health monitoring



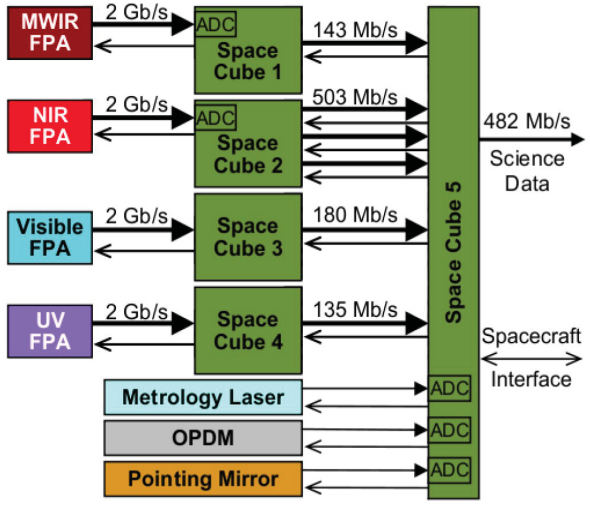
PanFTS UV-Vis ROIC



PanFTS at CLARS

Future Work

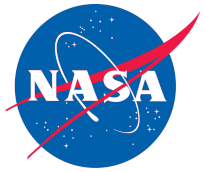
- Improved data transfer mechanism
  - TCP/IP Ethernet transfer still too CPU-intensive – need higher data rates
  - Considering moving to PCI-express interface
    - Development boards support connection
    - Removes load on CPU (core implemented mostly in HW)
- Further research into command and data handling system for space flight
  - Considering utilizing NASA Goddard SpaceCube as processing element per each FPA
  - Will use RadHard Virtex-5QV FPGA for processing incoming FPA data
  - Need lots of DDR memory to perform 256K-point FFT for each pixel



Potential PanFTS C&DH design

Conclusions

- PanFTS is a very ambitious undertaking
- IR signal chain is mostly complete
  - Demonstrated real-time IR imagery capture from Raytheon FPA
  - Produced per pixel spectra (comparable with established spectrometers)
  - Working on improving user control / interface with rest of instrument
- Next step include
  - Adding JPL-developed UV-Vis FPA to signal chain
  - Moving instrument to CLARS facility at Mt. Wilson
  - Working on improving data transfer mechanism
- A study is underway to identify instrument architecture for flight



Acknowledgments

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